said gate line, said light shielding film being connected to a potential so that an increase in parasitic capacitance between the light shielding film and the gate line is suppressed, a load amount on the gate line is suppressed, and a delay of gate potential is small;

said first semiconductive layer being located beneath the capacitance line and spaced from the lights shielding film by a gate insulating film and substantially in register with the light shielding film at a location not beneath the gate line;

a second substrate disposed opposite to said first substrate and with a predetermined interval; and

a liquid crystal layer held between said first substrate and said second substrate.

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2. (Amended) A liquid crystal display device according to claim 1, wherein said light shielding film is disposed between said substrate and said pixel transistor.

3. (Amended) A liquid crystal display device according to claim 1, wherein said light shielding film is disposed over said pixel transistor.

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4. A liquid crystal display device, comprising:

a first substrate and a second substrate opposite said first substrate with a liquid crystal layer held between said first and second substrate;

a light shielding film formed on said first substrate;

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a pixel transistor formed of a first silicon layer on said first substrate, said light shielding film for shielding against incident or scattered light;

a gate line;

a capacitance line, said capacitance line and said gate line formed of a second silicon layer;

a gate insulating film;

said light shielding film formed substantially beneath said first silicon layer and extending so as to terminate at a location which is not beneath said gate line, and disposed under said capacitance line, said light shielding film being connected to a fixed potential so that an increase in parasitic capacitance between the light shielding film and the gate line is suppressed, a load amount on said gate line is suppressed and a delay of gate potential is small.

5. The liquid crystal display device as set forth in claim 4, wherein said first silicon layer is located beneath said capacitance line and spaced from said light shielding film by a [first] gate insulating [layer] film and substantially in register with said light [emitting] shielding film at a location not beneath said gate line.

6. The liquid crystal display device as set forth in claim 5 wherein said light shielding film is made from a metal and is connected to a metal layer having a fixed potential.

Please add the following new claims:

7. (newly-added) A liquid crystal display device comprising:

a first substrate;

a semiconductor layer formed on said first substrate;

a gate line;

a capacitance line;

a light shielding film formed substantially beneath said semiconductor layer and extending so as to terminate at a location which is not beneath said gate line and disposed under said capacitance line, the light shielding film being connected to a fixed potential so that an increase in parasitic capacitance between the light shielding film and the gate line is suppressed, a load amount on the gate line is suppressed and a delay of gate potential is small;

the first semiconductor layer being located beneath the capacitance line and spaced from the light shielding film by a gate insulating film and substantially in register with the light shielding film at a location not beneath the gate line;

the light shielding film being made from metal and connected to a metal layer having a fixed potential.

8. (newly-added) The liquid crystal display device according to claim 7, wherein said first semiconductor layer is a silicon layer.

REMARKS

This is a full and timely response to the non-final Official

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